ABSTRACT

A probe card for a wafer test system is provided with a number of on board features enabling fan out of a test system controller channel to test multiple DUTs on a wafer, while limiting undesirable effects of fan out on test results. On board features of the probe card include one or more of the following: (a) DUT signal isolation provided by placing resistors in series with each DUT input to isolate failed DUTs; (b) DUT power isolation provided by switches, current limiters, or regulators in series with each DUT power pin to isolate the power supply from failed DUTs; (c) self test provided using an on board micro-controller or FPGA; (d) stacked daughter cards provided as part of the probe card to accommodate the additional on board test circuitry; and (e) use of a interface bus between a base PCB and daughter cards of the probe card, or the test system controller to minimize the number of interface wires between the base PCB and daughter cards or between the base PCB and the test system controller.